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(54) A low defect density composite dielectric

(57) A composite dielectric layer (102). A first layer (112) of the composite dielectric layer (102) has a small to no nitrogen concentration. A second layer (114) of the composite dielectric layer (102) has a larger nitrogen concentration (e.g., 5-15%). The composite dielectric layer (102) may be used as a thin gate dielectric wherein the second layer (114) is located adjacent a doped gate electrode (110) and has sufficient nitrogen concentration to stop penetration of dopant from the gate electrode (110) to the channel region (108). The first layer (112) is located between the second layer (114) and the channel region (108). The low nitrogen concentration of the first layer (112) is limited so as to not interfere with carrier mobility in the channel region (108).

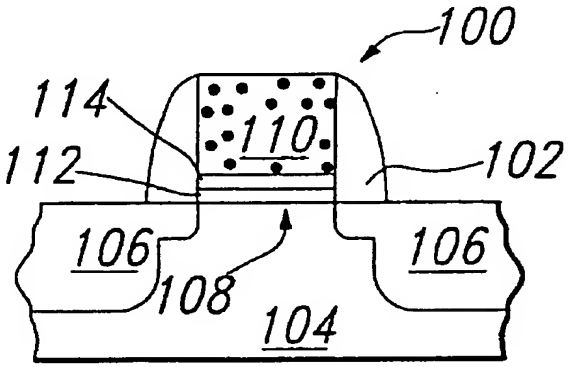

Fig.2

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Description

FIELD OF THE INVENTION

This invention generally relates to semiconductor devices and more specifically to a low defect density dielectrics.

BACKGROUND OF THE INVENTION

As semiconductor device geometries continue to shrink, dielectric layers such as those used to form gate dielectrics in MOSFET transistors need to become thinner to maintain transistor operating characteristics. FIG. 1 shows a p-type MOSFET transistor 10 having a thin gate dielectric 18. Gate dielectric 18 may, for example, comprise a thin layer of thermally grown silicon dioxide. Alternatively, for lower defect density, a composite of a thermally grown silicon dioxide with an overlying LPCVD silicon dioxide may be used. Gate dielectric 18 separates gate electrode 20 from the channel region 16. Gate electrode 20 typically comprises polysilicon doped for lower resistance. For a p-type MOSFET, boron is typically used to dope the gate electrode 20 and source/drain regions 14. However, due to the thinness of gate dielectric 18, during processing, boron from gate electrode 20 penetrates through the gate dielectric 18 into the channel region 16. Boron penetration into the channel impairs the performance of the transistor by degrading threshold voltage control, increasing off-state current leakage and decreasing reliability.

Several structures have been developed to stop boron penetration into the channel region. In one structure, the gate dielectric 18 is formed by thermally growing a silicon dioxide in a N_2O ambient to create an oxynitride. In another structure, the gate dielectric 18 is formed by depositing a nitrogen-doped oxide. Both structures use nitrogen at the gate dielectric/silicon interface to stop boron penetration. Unfortunately, the nitrogen levels required in the gate dielectric 18 to stop boron penetration degrade transistor carrier mobility. The nitrogen acts as a coulombic charge scattering center on the channel carriers, reducing their mobility. Thus, in determining the concentration of nitrogen to include in gate dielectric 18, there is a trade-off between blocking the boron penetration and maintaining high channel conductance.

SUMMARY OF THE INVENTION

The invention disclosed herein is a composite dielectric layer having low defect density. A first layer of the composite dielectric layer, for example, a LPCVD oxynitride or a nitrogen-doped oxide, contains a significant nitrogen concentration. The nitrogen concentration is sufficient to block dopants from penetrating through the dielectric layer. A second layer of the composite dielectric layer contains a significantly smaller nitrogen concentration (e.g., < 1%) or no nitrogen concentration at all. The second layer may be used to separate the first layer from another layer in the device that may be negatively affected by the higher nitrogen content (e.g., a channel region of a transistor for which nitrogen negatively impacts carrier mobility).

An advantage of the invention is providing a dielectric layer that can prevent boron penetration without impacting carrier mobility.

Another advantage of the invention is providing a dielectric layer having a low defect density and low leakage characteristics.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will now be further described by way of example, with reference to the accompanying drawings in which:

FIG. 1 is a cross-sectional diagram of a prior art p-type MOSFET illustrating boron penetration into the channel region;

FIG. 2 is a cross-sectional diagram of a p-type MOSFET including a gate dielectric according to the invention;

FIG. 3A is a cross-sectional diagram of the p-type MOSFET of FIG. 2 during fabrication;

FIG. 3B is a graph of nitrogen concentration versus depth within the dielectric layer of FIG. 3A; and

FIG. 4 is a cross-section diagram of capacitor including a dielectric layer according to the invention.

Corresponding numerals and symbols in the different figures refer to corresponding parts unless otherwise indicated.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The invention is a composite dielectric layer and will now be described in conjunction with a p-type MOSFET having a thin gate dielectric (i.e., < 60 Angstrams). However, it will be apparent to those skilled in the art that the dielectric layer is also applicable to other dielectric layers such as those used in inter-poly situations (e.g., DRAM stacked capacitors), thin film transistors, and other MOSFETS including those having thicker gate dielectrics (i.e., > 60 Angstrams).

A p-type MOSFET 100 having a thin composite gate dielectric 102 according to an embodiment of the invention is shown in FIG. 2. P-type source/drain regions 106 are located in semiconductor body 104. Gate electrode 110 is separated from channel region 108 by gate dielectric 102. Various conductive material choices for gate electrode 110 are known in the art. For example, gate electrode 110 may comprise a doped conductive material such as doped polysilicon. In order

to more fully demonstrate the advantages of the invention, the following discussion assumes that gate electrode 110 comprises polysilicon doped with boron. However, it should be noted that the invention is applicable to other dopants as well.

Gate dielectric 102 comprises at least two distinct layers 112 and 114. Dielectric layer 112 is located adjacent to channel region 108 and has little to no nitrogen content. On the other hand, dielectric layer 114 has a relatively high nitrogen content and is spaced away from channel region 108 by layer 112. Nitrogen retards the diffusion of boron dopants through a given layer. However, nitrogen also degrades carrier mobility when nitrogen is located at the dielectric layer/channel region interface. This is due to the fact that nitrogen at this interface acts as a coulombic charge scattering center on the carriers in the channel region, reducing carrier mobility. Thus, the nitrogen content in layer 114 is chosen to be sufficient to block the penetration of boron from gate electrode 110 to channel region 108 and the nitrogen content in layer 112 is chosen to minimize the influence of nitrogen on carrier mobility in the channel region. In the preferred embodiment, layer 112 has a nitrogen content less than 1% (e.g., 0- 1%) and layer 114 preferably has a nitrogen content in the range of 5-15%. However, it should be noted that a high percentage of nitrogen may alternatively be used. Thus, the trade-off required in prior art methods between boron blocking and carrier mobility is eliminated by having two distinct layers, one optimized for each factor.

A method for forming gate dielectric 102 will now be discussed. First, layer 112 is formed on the surface of semiconductor body as shown in FIG. 3A. Layer 112 contains little to no nitrogen (i.e., < 1%). For example, layer 112 may be a thermally grown silicon dioxide. Other examples for layer 112 will be apparent to those of ordinary skill in the art. For example, layer 112 may be grown in a variety of oxidizing ambients (e.g., O_2, N_2O, NO) and by a variety of reactors (furnace or single wafer reactor). The thickness of layer 112 depends on the total thickness of dielectric layer 102. Typical thicknesses for a thin gate dielectric may be in the range of 15-25 Angstrams. Next, layer 114, having a relatively high concentration of nitrogen is formed on layer 112. Layer 114 may, for example, be an oxynitride deposited by low pressure chemical vapor deposition (LPCVD) or a nitrogen doped high temperature oxide by conventional furnace or single wafer reactor. Again, the thickness of layer 114 depends on the total thickness desired for dielectric layer 102 with a typical thickness for a thin dielectric layer being in the range of 10-20 Angstrams. The overall thickness of gate dielectric 102 is determined by conventional means based on the rehired device parameters.

After the formation of layer 114, a light reoxidation may be performed to reduce stress between layers 112 and 114. If desired, the light reoxidation may be performed in a N_2O ambient (or N_2O and O_2 or NO) to improve reliability. However, the nitrogen content of layer 114 should be limited such that it is transparent to the oxidizing species during reoxidation so as not to introduce sufficient nitrogen quantities into layer 112 to harm mobilities and carrier transport properties. The final nitrogen concentration in layer 112 should remain less than 1%.

An example of a final nitrogen profile is illustrated in FIG. 3B. A nitrogen peak 120 of the oxide or oxynitride layer 114 provides boron blocking and has little influence on channel conduction properties. The peak nitrogen concentration may be in the range of 5-15%. A small percentage of nitrogen may also be found in layer 112 due to the light reoxidation step. The peak nitrogen level 122 in layer 112 is sufficient to improve reliability while having little effect on conduction by virtue of its small level (0.25-0.75%).

After the light reoxidation, conventional processing continues with the deposition of the gate electrode material, patterning and etch of the gate electrode material and gate dielectric 102, and formation of the source/drain regions 106. Following that, the source/drain regions and gate electrode may be silicided and interconnections between MOSFET 100 and other devices (not shown) may be formed.

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. For example, the gate dielectric structure is scalable to thicker films (i.e., > 60 Angstrams) and thin film transistors. Furthermore, the dielectric layer may be applied to DRAM capacitor applications, as shown in FIG. 4 wherein the dielectric layer 102 is placed between capacitor plates 130 and 132. Advantages for the DRAM capacitor application include low leakage and low defect density.

Claims

1. A composite dielectric layer comprising:

   a first dielectric layer having a nitrogen content less than 1%; and
   a second dielectric layer having a nitrogen content sufficient to substantially block penetration of dopants.

2. The composite dielectric layer of Claim 1, wherein said first dielectric layer is located adjacent a channel region of a transistor and said second dielectric layer is spaced from said channel region.

3. The composite dielectric layer of Claim 1 or Claim 2, wherein said first dielectric layer comprises silicon dioxide.

4. The composite dielectric layer of any of Claims 1 to 3, wherein said second dielectric layer comprises a nitrogen-doped oxide.

5. The composite dielectric layer of any of Claims 1 to 3, wherein said second dielectric layer comprises an oxynitride.

6. The composite dielectric layer of any of Claims 1 to 5, wherein said first dielectric layer has a thickness of the order of 15-25 Angstrams.

7. The composite dielectric layer of any of Claims 1 to 6, wherein said second dielectric layer has a thickness of the order of 10-20 Angstrams.

8. The composite dielectric layer of any of Claims 1 to 7, wherein said second dielectric layer has a nitrogen concentration substantially in the range of 5-15%.

9. The composite dielectric layer of any of Claims 1 to 8, wherein said first dielectric layer is located substantially between a first polysilicon layer and said second dielectric layer, and wherein said second dielectric layer is located substantially between said first dielectric layer and a second polysilicon layer.

10. The composite dielectric layer of Claim 1 or any of Claims 3 to 9, wherein said first and second dielectric layers are located between first and second plates of a capacitor.

11. A MOSFET transistor, comprising:

a first current guiding region and a second current guiding region formed in a semiconductor body;
a channel region formed substantially between said first and second current guiding regions;
a doped control region disposed substantially over said channel region; and
a dielectric region disposed between said doped control region and said channel region, said dielectric comprising:
a first layer located adjacent said channel region and having a sufficiently small nitrogen concentration that carrier mobility in said channel region is not influenced; and
a second layer located adjacent said control region and having a nitrogen concentration sufficient to substantially block the penetration of dopants from said doped control region.

12. The transistor of Claim 11, wherein said first layer contains a nitrogen concentration substantially between 0 and 1%.

13. The transistor of Claim 11 or Claim 12, wherein said second layer has a nitrogen concentration substantially between 5 and 15%.

14. The transistor of any of Claims 11 to 13, wherein said doped control region is doped with boron.

15. The transistor of any of Claims 11 to 14, wherein said first layer comprises silicon dioxide.

16. The transistor of any of Claims 11 to 15, wherein said second layer comprises a nitrogen-doped oxide.

17. The transistor of any of Claims 11 to 15, wherein said second layer comprises an oxynitride.

18. A method of forming a composite dielectric layer, comprising the steps of:

thermally growing a layer of silicon dioxide on a semiconductor body; and
forming a nitrogen-containing dielectric layer on said layer of silicon dioxide, such that said nitrogen-containing layer has a nitrogen concentration sufficient to substantially block the penetration of dopants.

19. The method of Claim 18, further comprising the step of lightly reoxidizing said layer of silicon dioxide and said nitrogen-containing layer to reduce stress.

20. The method of Claim 18 or Claim 19, wherein said step of forming said nitrogen-containing layer comprises the step of depositing a nitrogen-doped oxide layer.

21. The method of Claims 18 or Claim 19, wherein said step of forming said nitrogen-containing layer comprises the step of thermally growing an oxide layer in a N_2O ambient.

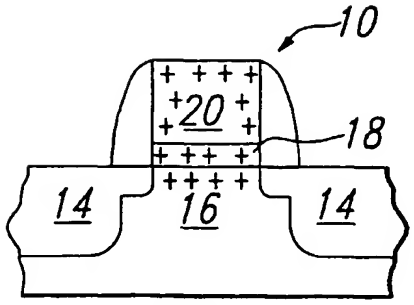

Fig.1

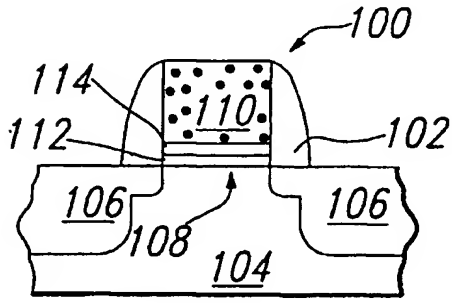

Fig.2

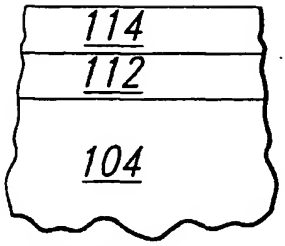

Fig.3A

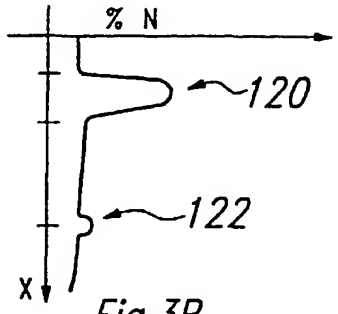

Fig.3B

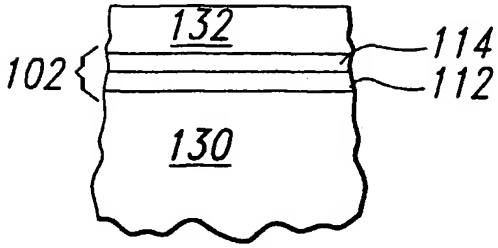

Fig.4